

NDS9936

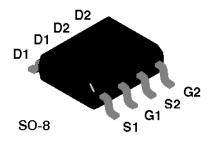
Dual N-Channel Enhancement Mode Field Effect Transistor

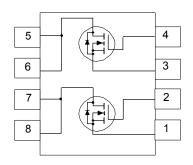
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC/DC conversion, disk drive motor control, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5A, 30V. $R_{DS(ON)} = 0.05\Omega$ @ $V_{GS} = 10V$.
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_a = 25°C unless otherwise noted

ymbol	Parameter	NDS9936	Units
DSS	Drain-Source Voltage	30	V
/ GSS	Gate-Source Voltage	± 20	V
)	Drain Current - Continuous @ T _A = 25°C (Note 1a)	± 5.0	А
	- Continuous @ T _A = 70°C (Note 1a)	± 4.0	
	- Pulsed @ T _A = 25°C	± 40	
P_{D}	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
,T _{STG}	Operating and Storage Temperature Range	-55 to 150	°C
HERMA	L CHARACTERISTICS		
θЈΑ	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
θJC	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS	·					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$				2	μΑ
			T _J = 55°C			20	μA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	·			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAR	RACTERISTICS (Note 2)						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.4	3	V
			T _J =125°C	0.7	1.1	2.2	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$			0.044	0.05	Ω
			T _J =125°C		0.066	0.1	
		$V_{GS} = 4.5 \text{ V}, I_{D} = 3.9 \text{ A}$			0.066	0.08	-
			T _J =125°C		0.099	0.16	
I _{D(on)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		40			Α
		$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}$		20			
9 _{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 3.5 \text{ A}$		3	8		S
DYNAMIC	CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, \ V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$			525		pF
C _{oss}	Output Capacitance				315		pF
C _{rss}	Reverse Transfer Capacitance				185		pF
SWITCHI	NG CHARACTERISTICS (Note 2)						
t _{D(ON)}	Tum - On Delay Time	$V_{DD} = 15 \text{ V}, \ I_{D} = 1 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$			12	30	ns
ţ	Turn - On Rise Time				10	25	ns
t _{D(OFF)}	Turn - Off Delay Time				25	50	ns
ţ,	Turn - Off Fall Time				10	50	ns
Q_g	Total Gate Charge	V _{DS} = 15 V,			17	35	nC
Q_{gs}	Gate-Source Charge	I _D = 5 A, V _{GS} = 10 V			1.5		nC
Q_{gd}	Gate-Drain Charge				3.7		nC

Electrical Characteristics (T _A = 25°C unless otherwise noted)							
Symbol	Parameter Conditions		Min	Тур	Max	Units	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
Is	Maximum Continuos Drain-Source Diode Forward Current				1.7	Α	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.7 A (Note 2)		0.78	1.2	V	
t,,	Reverse Recovery Time	$V_{GS} = 0V, I_{F} = 5 A, dI_{F}/dt = 100 A/\mu s$		70	160	ns	

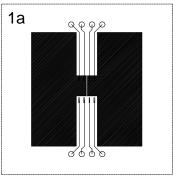
Notes:

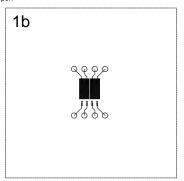
1. R_{BJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BJC} is guaranteed by design while R_{BCA} is determined by the user's board design.

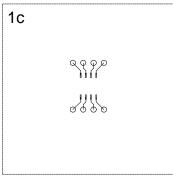
$$P_D(t) = \frac{T_{J} - T_A}{R_{\theta J} \, \underline{A}(t)} = \frac{T_{J} - T_A}{R_{\theta J} \, \underline{d} \, R_{\theta C} \, \underline{d}(t)} = I_D^2(t) \times R_{DS(ON)} \, \underline{\mathfrak{G}}_{T_J}$$

Typical R_{BJA} for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $\leq 300 \mu s,$ Duty Cycle $\leq 2.0 \%.$

Typical Electrical Characteristics

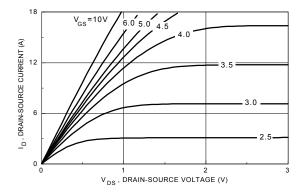


Figure 1. On-Region Characteristics.

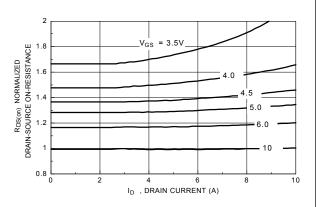


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

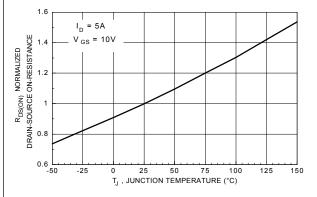


Figure 3. On-Resistance Variation with Temperature.

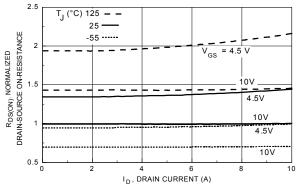


Figure 4. On-Resistance Variation with Drain Current and Temperature.

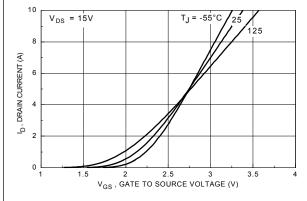


Figure 5. Transfer Characteristics.

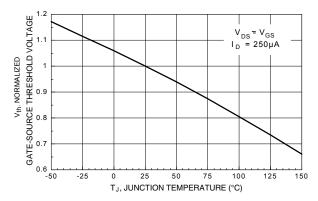


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

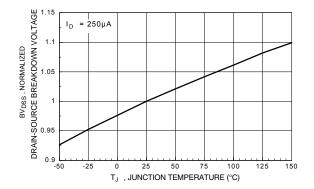


Figure 7. Breakdown Voltage Variation with Temperature.

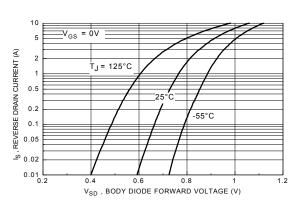


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

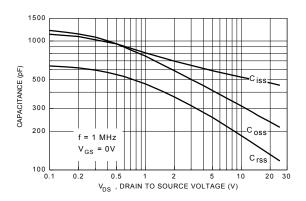


Figure 9. Capacitance Characteristics.

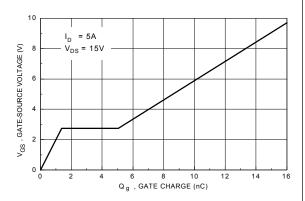


Figure 10. Gate Charge Characteristics.

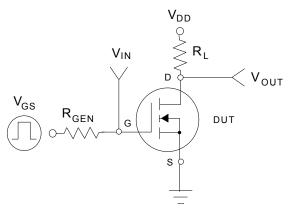


Figure 11. Switching Test Circuit.

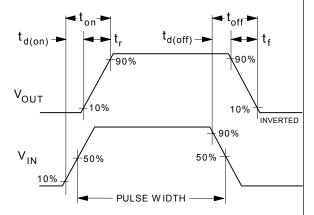
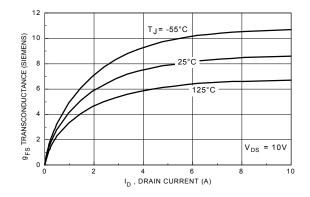


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)



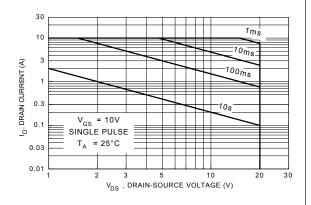


Figure 13. Transconductance Variation with Drain **Current and Temperature.**

Figure 14. Maximum Safe Operating Area.

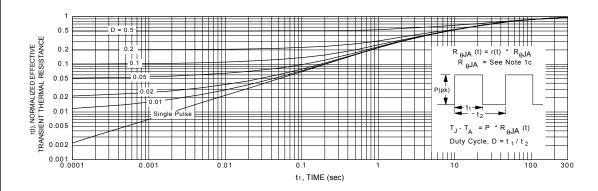


Figure 15. Transient Thermal Response Curve.

Themal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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